

N.B.: (1) Question No. 1 is **Compulsory**.

- (2) Attempt any **three** questions out of the remaining **five**.
- (3) Each question carries 20 marks and sub-question carry equal marks.
- (4) Assume suitable data if required.
1. (a) (I) Convert decimal number **0.875** in the binary form. (5)
 (II) Convert binary number **1010101** in the decimal form.
 (III) Find two's complement of the number **011101000**
 (IV) Convert decimal number **346** into octal form.
 (V) Perform the operation (**57 – 32**) using two's complement method. Use 8-bit representation of numbers.
 - (b) Implement the functions F1 and F2 using PLA with 3 inputs, 3 product terms, 2 outputs. (5)
 $F1 = \sum m(4, 5, 7)$, $F2 = \sum m(4, 5, 6)$
 - (c) Convert SR Flip Flop to D Flip Flop. (5)
 - (d) Draw gate level diagram of 1 : 4 De-multiplexer having active low outputs, chip enable and explain its operation. (5)
 2. (a) Design a Mod 5 lockout free synchronous up counter using JKMS Flip Flops. (10)
 - (b) Design 5-bit comparator using only one 4-bit comparator IC 7485 and explain its operation. (10)
 3. (a) Write short notes on (I) CPLD architecture (II) Data types in Verilog. (10)
 - (b) Draw block diagram of synchronous counter IC 74163, explain its operation and Design Mod-13 counter using this IC. (10)
 4. (a) Discuss Interfacing CMOS to TTL and TTL to CMOS logic families. (10)
 - (b) Design a Mealy type overlapping serial sequence detector using D flip flops to detect the sequence 01101. (10)
 - 5 (a) Draw TTL two input NAND gate and explain its operation. (10)
 - (b) Write short notes on (I) De-Morgan Theorems (II) Hamming Code (10)
 6. (a) Implement the function using only one 4:1 multiplexer and few gates; (10)
 $Y = F(A, B, C, D) = \sum m(0, 1, 6, 12, 13, 14, 15)$
 - (b) Write a Verilog code for Full Adder using CASE statement. (10)
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